

REMARKS

Claims 1-4 were previously canceled and claims 5-7 were presented for examination. In the 06/08/2004 final Office Action, the Examiner rejected claims 5-7 under 35 U.S.C. §102(e) as anticipated by Taussig (US Patent No. 6,552,409). Carl Taussig is an inventor named in US Patent No. 6,552,409 and an inventor named in the present application. The Examiner stated that the rejection might be overcome through a 37 CFR 1.132 declaration that an inventor of this application exclusively originated the subject matter disclosed in that part of the Taussig reference referred to by the examiner in the June 8, 2004 Office Action.

In the specification, three paragraphs have been amended to include the US patent serial number of the reference noted in the specification and two of the three paragraphs have been amended to correct minor editorial problems. Claims 5-7 have been amended to correct minor editorial problems. Dependent claims 8-14 are new.


Included as part of this Response is EXHIBIT 1 - a declaration from inventor Carl Taussig unequivocally establishing that Carl Taussig exclusively originated the subject matter disclosed in that part of the Taussig reference referred to by the examiner in the June 8, 2004 Office Action. In view of the foregoing, it is submitted that all pending claims, namely claims 8-14, are in condition for allowance. Reconsideration of the rejections is requested. Allowance is earnestly solicited at the earliest possible date.

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Respectfully submitted,

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EXHIBIT 1

37 CFR 1.132 DECLARATION OF CARL TAUSSIG

1. I, Carl Taussig, declare from first hand knowledge as follows.
2. I am one of the two named inventors in the patent application having U.S. Application No. 10/696,992.
3. I have reviewed pending claims 5-7, which are:
5. A digital circuitry system comprising: a memory module having a plurality of stackable cross-point memory arrays stacked so as to have interconnection in a unitary package; and a plurality of conductive pads, said conductive pads adapted for providing said interconnection of said stacked cross-point memory arrays through a patterned waffle structure.
6. The digital circuitry system as claimed in claim 5, wherein said patterned waffle structure of said conductive pads is formed from at least two separately patterned groupings of layered materials which are combined together, in substantially the same planar direction, at a substantially orthogonal juxtaposition.
7. The digital circuitry system as claimed in claim 6, wherein said at least two separately patterned groupings of layered materials are formed from the application of at least one thin film on a flexible substrate.
4. I have reviewed the June 8, 2004 Office Action, including the rejection grounds statement which reads: *Claims 5-7 are rejected under 35 USC 102(e) as being anticipated by Taussig et al. US 6,552,409. Taussig discloses a digital circuitry system including memory module having a plurality of stackable cross-point memory arrays stacked so as to have interconnection in a unitary package, a plurality of conductive pads, the conductive pads adapted for providing the interconnection of the stacked cross-point memory arrays through a patterned waffle structure, wherein the patterned waffle structure of the conductive pads is formed from at least two separately patterned groupings (802, 804) of layered materials which are combined together, wherein at least one of the layered materials is formed from the application of at least one thin film on a flexible substrate, and combining together include in substantially the same planar direction, at a substantially orthogonal juxtaposition (see figs. 16-25 and related text).*
5. I have reviewed that part of the Taussig reference referred to by the examiner in the June 8, 2004 Office Action.
6. Unequivocally, I solely conceived the subject matter disclosed in that part of the Taussig reference referred to by the examiner in the June 8, 2004 Office Action. In other words, I exclusively originated the subject matter disclosed in that part of the Taussig reference referred to by the examiner in the June 8, 2004 Office Action and it is my own work.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date:

26-Aug-04

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